CDS - erases' picture frame - raw noise

TP 13 on Jade card = Agnd

took CDS noise frame

frame time 1.39264 s, frame index 3, total time 18.77s, data write time 1.95 s, exp time counter 0,

15:17:24 CDS noise in full frame
resets 1, reads 2, ramps 2, groups 1, drops 0

CDSnoise1.fits display -1125.8 - +904 counts

\Data\HxRG\H2RG-ASIC-000-0-000\CDS Noise

folder 20090731 (date) 151724 (time)

stores under frames and folder Result

$V = Q/C$

didn't name it CDS Noise1

need to look @ bands though?

has some complete fits header

(empty buffer DV though)

CM fixed external power supply

tested D = 7, Cryo_Septup.mcd CDS
no ref pix sub-

against a USB - much better.

Saturday 1 Aug 2009 3PM - pump still off
The inner + outer totally empty, Inner warm ~ room
∃ a leak (+ NO Getter) + Start Pump
then opened down valve, P ↑ 300μ Hg - then decrease

Note: raw noise eliminated (to great extent) by external 5V P. supply ⇒ Jade + ASIC have little & any voltage regulation built into them!

Look @ vertical graph in DSA - focuss on each of the 32 outputs - RMS Noise = ~~P~~ P-P/5
Check out a sample of them Gain = 7 ⇒ 12 dB ⇒ × 4.0
⇒ (11,3/4) × 4.5 = ~~12~~ 12.7 μV/ADU × 40×10^{-15} ÷ 1.6×10^{-19} = 3.2 e⁻/ADU

using Cryo_Stup.mcd (Christoff c

X "Channel"	RMS (ADU)	μV	e⁻	P-P (ADU)	
929				40	no ref pix s
602				100	
24				30	
96			65	100	
151	8	104	26	40	
1830	5	64	16	25	~ lowest
1507	24	312	78	120	~ highest

Read noise varies channel to channel from 64 μV (~16 e⁻) to 312 μV (~78 e⁻)

Dewar full @ 4PM
~~Should~~ slow down cooling for HgCdTe devices — explosion

Sunday 2 Aug 2009 7AM
Outer empty; Inner ~ 1-2" LN2 fill both

Monday 9:30 am 3 Aug 2009

Outer empty, inner almost full — fill both.
Odd-Even effect for these fpa_001-01-fi

Column	X	p-p ADU		
FRIDAY 1 (L)	28	50		62 ← D=8
2	87	100 LCD=7		75
3	160	40 Cin low		50-60 Cin high
4	215	100-150		100 MONDAY with
5	283	30		50 TIS
6	351	100-150		75-87 S/W
7	411	30 (ω2 ex cuts 250)		50-62
8	470	120		
9	538	40		
10	611	150		
11	665	25		
12	734	120		
13	793	45		
14	857	110		
15	916	30		

19	1184	30 (50)
20	1243	70 (100)
21	1302	30
22	1371	90
23	1439	30 (w lot of drifts)
24	1507	120
25	1571	50
26	1630	100
27	1698	30 w 1 excursion to 200, 1 to 150
28	1753	100
29	1835	25 w 1 excursion to 150
30	1800	60 w 7 excursions to 200
31	1949	30
32	2008	100-110

Hex Jade2 ASIC 1

x	4000	4001	4002	4003	4004	4005	4006	x 4007
x	4008	4009	400A	400B	400C	400D	400E	400F
x	4010	4011 # ~~checkpts~~	4012 # chan/output	4013	4014	4015	4016	4017
x	4018	4019	401A	401B	401C	401D	401E	401F
x	4020	4021	4022	4023				

Bill Sugg. use IDL to control HXRG Testing Software

Jade Board - unplugged AC power, lights stayed on. unplugged USB, went out.

add Jade (back) powered by USB } power cycle disconnect both

HAC on

~~Hys Config~~ HXRG init - first time Check both download JAE + Register

Later just JADE2 Reg (+ st d.t. MCD)

React per frame better cryo.
(per raw if adjustbias).

unbuf. diff.

Act config – single. fast acquire

same word.

look @ power readback jitter

(check proper jumper).

W2 closer to middle — W3 one connects Agnd Dgnd, other removed for ext. pwr supply

green box – ASIC avail pcn.
= green circle

Changed V_1 Vrefpwr
V_3 Padp
V_2 Gndpin
V_4 Gndpin.

voltages and currents look ok ~5 V.

pwr

Act config pwr.

ASIC view floorpl.

floorpl

click floor plan voltage

parked

Vref pwr comes up

reset per raw

& look for effect

parked

@ 1.6V – failed

if 6812 setting wrong; ASIC literature.

V1 Vref,warm V3 Padp

V2 Vref,1 V4 IaTca

~1.6 D~2 mV g=0.7 D=0

single frame ~32000 ADU
but no pic. frame.

D=8 gx4 Vref,warm 1.52 VRef,1 1.607
correctly.

• offsets changed quite a bit •

Vref,warm 1.4115
Vref,warm 1.3431 → 1.6070 Vref,1 (rail bottom end bat on scale single frame.
+ Tdewar affects offsets. –
+ may be new power supply.

Our noise with gain code of 8 is ~600 ADU
~40 e⁻

D=7 gx4 – redid (14:39)
w Cin=low.

found that displayed image when read data was ~~same~~ 32-bit integer signed

so we saved, and moved to results directory to compare with the CDS frame offset by 32768

decided to put shield over Cable fm. dewar to JADE

IDL start –

in IDL command line starts w HXRG

DMA | Autowrite

Systematic –

V1 → inverting input of S/H

Vrefmain on 3 of Vi } leave in
Vpadp on V2 } overwrite mode

adjust VrefMain until ∅ on image (32768)

VRef Main	
1.5112	8–10,000 ADU
1.5152	6000 dark splotch
1.5230	5000 "
1.5327	4000
1.5738	1000
1.5855	700
1.5953	100
⇒ 1.6051 ←	maybe a bit more
1.7009	0's everywhere

$\Delta = 100$ mV → $\Delta \approx -1000$

Now with this VRefMAIN.

Change V_2 to I_n param.

1.7009 stripes – (993, 1351) 11,171

1.9101 0's.
1.8710 500 but some channels already failed
InPcommon 1.87V except first column + bottom.

Set InPcom 1.80084

Two pairs V1, V3 fed − V4, V2 fed +
pad pair of these choose V2.

InpcomV1
Vref1 (V3) set to average Inpcom

Couldn't get Vref1 to display

Do use Vref2 = 1.8084

set Vrefmain 1.6051
found Vref1 set to 1.8084

Try
VREFMAIN = 1.7067
mostly 32768

VREFMAIN 1.6051 mostly 32768
Vref1 1.7087

totally changed — V2 to Inpcom
Vrefmain 1.8084.

Tuesday 4 August 2009 Something in the IDE/IDL/HAL/Jade/SidecarASIC is going bad. Kind of like Windows - eventually it goes bad & one has to reboot). Suspect SidecarASIC has been corrupted. ∴ Re-upload code to ASIC & try again. This time check 32768 & 65535 ADU as well as zero ADU. First measure

PadP, then measure It Common Then check PadP again Then use Vref1 (instead of V Main) to measure the PadP voltage (~1.6 V)

Note: should have Rectangles ~~IDE~~ surrounding "DM + "Auto Write" on the IDE GUI "Auto Write" mea when changing VRefMain (Channel 2) - IDE writes it soon as you stop clicking. Never hit the "Load" but This will write every thing to some default va which may be different than you want

Note: The 4 voltages input to the S/A with gain amplifier are configured →

$$V_{out} = [(V_2 - V_4) - (V_1 - V_3)] \times g$$

"+" input "−" input

i.e, if we set $V_4 = V_2$ (PadP, the array out put volt + $V_3 = V_1$ (ImP common, the single refe voltage for all the up to 32, array outputs)

Then the "+" input & "−" inputs should be close to zero & not railed?

Note: Since our bias voltages are only in the range 0 - 3.3 V, I think zero volts is railed

∴ we should actually shoot for +1 V! I (I speculate that our "crazy condition" happens when one or more FETs get "railed" - to unrail them we ha to remove power to the ASIC + start over (ie. re-boot)

X Fer LN2 Plug in USB + DC power @ 1 AM
Using IDL GUI X11.2 (IDL v. 6.4, IDE v. 2.1)
Stop IDL/GUI + IDE start IDE first
IDE selection mikes directory (HxRG) file HxRG.sol
2= VRefMain 0 = VRef1
use IDE to start HAL server (nothing else, except to change, i.e. VRefMain + VRef1)

0 min later - play back in - 2 lights, one dim
unload Jade Firmware (45 s) + Registers from "Mike"
directory (renamed HxRG) "INITIALIZE" again
- lights + one flashing (using 1 ADC / output
Change # Outputs to 32, Gain Code 8 (gx4, large Cin)
According to Mike - should Reset by Read, when adjusting
VRefMain - i.e. preamp capacitors leak
Pad V2 V1, 3+4 VRefMain @ 1.34V 20,000 ADU
VRefMain (2) Dark blemish
1.34 V 20,000 ADU
1.60 V ~400 ADU (as before) 20,000 ADU / .26 V = 80,000 ADU / 1V
Take CDS here looks OK
1.34 V 18,000 (~20,000)
1.21 V (should be 32,000) 29,000
0.8 V 59,000 There are ~50 pix near
top @ 65,535 (ie railed)
1.6V (check zero) ~500 (some railed @ zero)
Now repeat with InP Common on V2
1.6 V 19,000 (X=1120)
1.8 V 4000 (small range, except zero near bottom
1.1 V 56,000
Now put (V2 = Pad V1 = InP Common
V4 = VRefMain) V3 = VRef1
Set VRefMain = 1.5V VRef1 = 1.75V
VRefMain VRef1
1.5 1.75 Blemish @ 32,000 RMS Noise ~80-100 ADU
CDS image looks reasonable (except They add
32,768 to the CDS image
Go to 4-output mode - blemish still @ 32,000
P-P Noise 5
1-512, 513-1024, 1025-1768 1768-2048
35 40 40 30
Change to Gain Code 7 (same gain, small In Put Cap)
Blemish @ 31,000, OK
40 50 50 30
Change to Gain Code 10 (15 dB, large Cinput
Blemish @ 31,000 - OK!
50 62 70 35 ← avoiding row noise
Gain Code 12 (18 dB large Cin) Blemish @ 31,000!
75 90 90 60
Gain Code 13 (21 dB large Cin) 9x11.3 Blemish @ 30,000
120 130 130 80
No CDS Noise - It seems as written - only non-

Excellent Noise analysis. Looking @ some FITS headers — it seems the gain might not have been right — I'll acquire a new gain code 13 CDS image & measure noise

1–512 1500–2048
120 75 about the same

Now GainCode 15 (largest) 27 dB + large C_{in}

Blemish @ 28,000
180 200 180 120

Header said ASIC GainCode 13! — probably wrong!
Take another CDS without changing any thing
Now Fits header says ASIC GainCode = 15! Noise is same (120 ADU p-p for 4th "channel columns 1500–2048)

Now GainCode 0 (-3 dB, small C_{in}), blemish @ 32,000+
13 12 13 13 all 4 "channels" = outputs the same A/D noise = 13/5 = 2.6 ADU's for 2 samples
2.6 / 1.4 = 1.9 rms ADU per sample

"Blemish" contrast = 550 ADU @ g x 0.7 } 22.6/1.7 = 32
1700 x 10 @ g x 22.6
~~1700/550 ~ 3!~~ 17000/550 = 31!

Gain working
@ g x 22.6 1 ADU = $3.2e^- \times \frac{4}{22.6} = 0.57e^-$

3/4 of array read noise $\frac{190}{5} \times .57 = 22e^-$
best 1/4 $512/5 \times .57 = 14e^-$

Back to gain code 15 3:26 PM. Delete first directory
Go to 32 output mode / Blemish 25,000 (vs 27,000 in 4 output mode) *32
noise in very last output ~300 ADU p-p 2.5 times higher noise #28 ~350 #26 ~250 #10 ~500
output #1 (col 28) 220 ADU p-p col 591

Noise in 32 output much higher!

Try 1-output mode (42s IT time) blemish @ 25,000 ADU
p-p noise Vertical 160 ADU Horizontal 150 ADU
Horizontal is 6% quieter than Vertical

ll be hard to use ref. pix to correct anything!
back to 4-output mode — check out Ref Pix Theo
blemish @ 26,000 ADU
Note: Ref pixels railed @ 0 ADU — need to increase
input (decrease V Ref Main #2)

Reduce V Ref Main 1.50 → 1.45 V take image
Blemish @ 49,000 ADU many pixel > 65,535 —
V Ref Main 1.48 CDS image
Blemish @ 39,000. Max pixel ~ 30-40 pix @ 65,535
Ref pix @ ~10,000 ADU
Measure noise in horizontal direction
Col 1-512 513-1024 1025-1536 1537-2048
100 170 170 80) somewhat smaller!
Now reset per row Preamp (was per frame) (blemish 35,000)
More high-freq row noise)
160 160 160 100 (180 vertical!)
Back to Reset (preamp) per frame + new preamp KTC removal
210 230 220 170 (190 vertical)
KTC removal fails — "clean" noise — back to un removal
Go from Unbuffered Mode to Buffered Mode (with current source)
Railed @ 65,535 — can't see picture frame or blemish
Go from "overwrite with" V1, V2, V3, V4 to
"Single Ended — V Ref Main"
Railed at zero! Try "Differential — In P common"
blemish @ 39,000 — OK
130 180 180 110 (130 vertical)
Some what higher than "Best" above 10-20%
5:10 PM Stop

Wednesday Aug 5, 2009

topped off dewar 10:15 am

Bill wants to warm up replace ASIC
and board mux to one of 2
arrays

first Christoff w/wo ref pix

D=8, no ref pix sub, F2 2.7855
DATA Aug 5