Spatial Distributions of Hole Traps, and Image Latency in InSb Focal Plane Arrays

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ABSTRACT

Spatial distributions of hole trap sites on a quasipixel level in InSb arrays for SIRTF are examined. The dependence of flux, fluence, and applied bias on image latency is investigated, and experimental results are presented and discussed. Models of linearity and capacitance are compared with experimental results. We find increasing the depletion width in a light exposed pixel by larger reverse biasing decreases the trapped charge (or latency) in that pixel by factors of ~3. Assumed pixel geometries lead to an apparent spatial density of active trap sites that falls quickly with distance from the implants.

Keywords: InSb, Latent Image, Charge Trapping, Hole Trap, Linearity, Capacitance.

1. INTRODUCTION

1.1. Overview

The phenomenon of latent charge in many imaging photo-detectors is an issue of considerable importance. The development of new low noise, low dark current, imaging semiconductor arrays has led to the possibility of photometry on the 1-2% level*. For such accurate photometry, issues of missing photo-excited charge become highly relevant. We consider this issue for photo-voltaic Indium Antimonide or InSb diodes in 2-dimensional arrays.

In these arrays, photons with energies greater then 235meV, λ <5.3μm, produce electron hole pairs†. The holes diffuse through the detector until they encounter the diode's depletion region, where they are captured by the p-n junction's electric field. The holes accumulate in the p-type material and are eventually counted in the detecting circuit.

A latent charge is a charge that is temporarily trapped. A latent image results when these trapped charges become mobile and are counted in the detecting circuit.

Image latency impacts good photometry by removing photo-charge that should have been counted in the original image and releasing it at a later, and sometimes inopportune, moment. In astronomy, for example, when imaging a star and subsequently imaging a faint object at the same location on the array, latent charge from the star's image can be released into the new object's image. The result is less apparent signal from the star and too much apparent signal from the object.

Work conducted by Solomon on a previous generation of InSb arrays concluded holes were trapped by impurity sites in the SiO_x passivation near the frontside of the detector, and tunneling from these sites back into the InSb resulted in latent charge.[4] It is believed by the authors that any trap sites that exist in the depleted bulk of the diode's p-n junction do not significantly contribute to the charge trapping observed in this work.

This work began as part of the IRAC requirements for SIRTF. The detector used in this work is from a design identical to the Insb's used in the IRAC instrument. The latent image requirements for IRAC and the test performance of the IRAC InSb arrays are given in table 12 of appendix C.

The goal of this research is three-fold: To measure the spatial trap density, to describe the behavior of latent charge under variations of several dependant variables, and to offer possible strategies for minimizing latent effects.

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*The Space Infrared Telescope Facility's IRAC channels at 3.6μm and 4.5μm use InSb detectors, and quote sensitivities at the 5σ level for a ~6μJy point source integrated over ~100 seconds.

†The minimum photon energy needed to generate an electron hole pair is determined by the bandgap of InSb, which is 235 meV at near zero temperatures.

1.2. The Indium Antimonide FPA

The experiments described in the following pages were performed on an InSb focal plane array, Raytheon part number SCA41626. The detector consists of an array of photo-voltaic diodes operating in the reverse bias mode. The array measures 256x256 pixels square, with a 30μm pixel pitch. Individual pixels consist of a bulk InSb layer thinned to $\sim$7μm and low doped ($2x10^{14}cm^{-3}$) with donors (n-type), and a high doped($\sim10^{18}cm^{-3}$) rectangular acceptor (p-type) implant[6] measuring $\sim$22μm on a side and $\sim$1.0μm deep.[2] At zero bias the p-n junction creates a depletion region $\sim$1.5μm wide. The depletion region extends almost exclusively into the n-type material due to the relative doping concentrations between the p-type and n-type materials.[8] The potential difference across the p-n junction due to the relative doping concentrations is known as the detector's built-in bias, it is approximately[3] 234mV. See Figure 1.

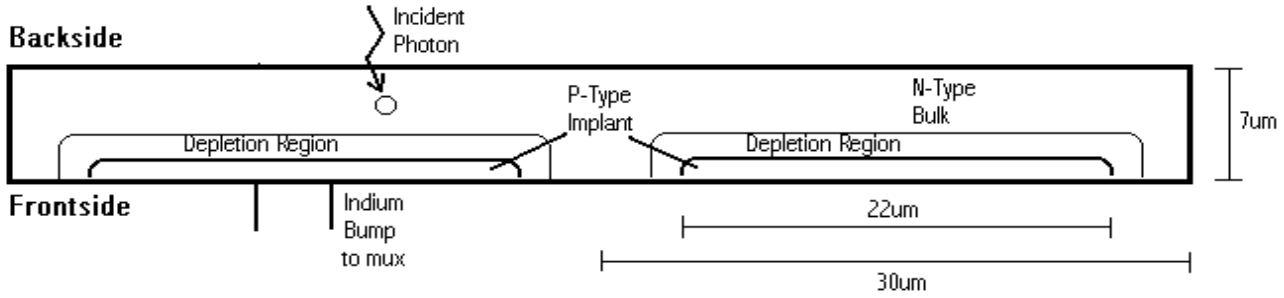

Figure 1. Detector Layout.

The multiplexing electronics, or mux, is connected to the detecting semiconductor via indium bumps and metal contacts. It is a Hughes/Raytheon 744 series.[9] Clocking of shift registers electronically selects one pixel. Its accumulated charge is read via source follower FETs. The output voltage from the pixel is buffered by an output FET which is sampled by our data system. The mux introduces changes to the detector bias when the FETs are turned off and on. This is due to capacitative coupling and is known as charge dump.[9] For 450mV of external reverse bias, the actual reverse bias applied to the diode is approximately 300mV (during integration and reading). As the diode integrates charge it debiases.

1.3. The Dewar

The cryogenic dewar used in the experiment was built by George Gull (Electromechanical Design Inc). The construction of the dewar isolates the InSb detector from room atmosphere and temperature by a vacuum, a liquid nitrogen cooled shield, and a liquid helium cooled shield. The InSb detector is mounted on a fiberglass pc board and is thermally isolated from the helium surface with nylon washers. Resistor heaters are used to obtain detector operating temperatures in the 5.5K to 40K range. A filter wheel, housing a variety of near infrared filters, is mounted to the helium shield. A computer controlled motor turns the filter wheel for selecting filters. A 3.3μm broadband filter is used for all the latent image data. The filter's bandpass is approximately 300nm FWHM. Between broadband filters on the filter wheel is cold, dark, and opaque metal. This space between filters is used to block photons, allowing one a virtually source-less background while still being relatively close, spatially, to the source filter. The filter wheel rotates from the broadband filter to the cd' (cold dark spot) in $\sim$0.5 seconds.

1.4. Data Collection System

A rack mount Pentium computer running Linux is utilized for data acquisition. Data acquisition is controlled by software developed by researchers at the University of Rochester over several years. The amount of applied reverse bias voltage to the semiconductor is controlled by a D/A converter under software control. The computer converts analog input voltages to digital signals, (ADU's), via A/D converters.

2. EXPERIMENTAL PROCEDURES

2.1. Latent Image Experiments

A 3.3μm source image followed by a series of cold dark latent images comprise a latent test run. For all cd' latent images, the integration time was 20 seconds and the applied reverse bias was the same as the preceding source frame. The runs began and ended on the cd' blocking filter. For each applied bias the latent runs were identical.

In order to test over a wide range of source flux in each test run, the filter wheel was positioned at one edge of the 3.3μm filter. The position was chosen to minimize the flux ($\sim$14e$^-$/sec) on the left side of the array (near column 1), and the maximum flux on the right side of the array (near column 256). The average maximum flux used for all the experiments was approximately 12,500 e$^-$/sec (discharging the InSb diode at 30mV/sec on average). The dark cd' position ensured the array experienced no higher fluxes when moving from the 3.3μm filter.

A run began by imaging on the dark (cd') position of the filter wheel. Once it was clear no latent signal was present, (typically after a few minutes), the filter wheel was moved directly to the source location and a source image was taken. The filter wheel was then moved directly back to the cd' position, where 10 successive latent images, described above, were taken. See Figure 2.

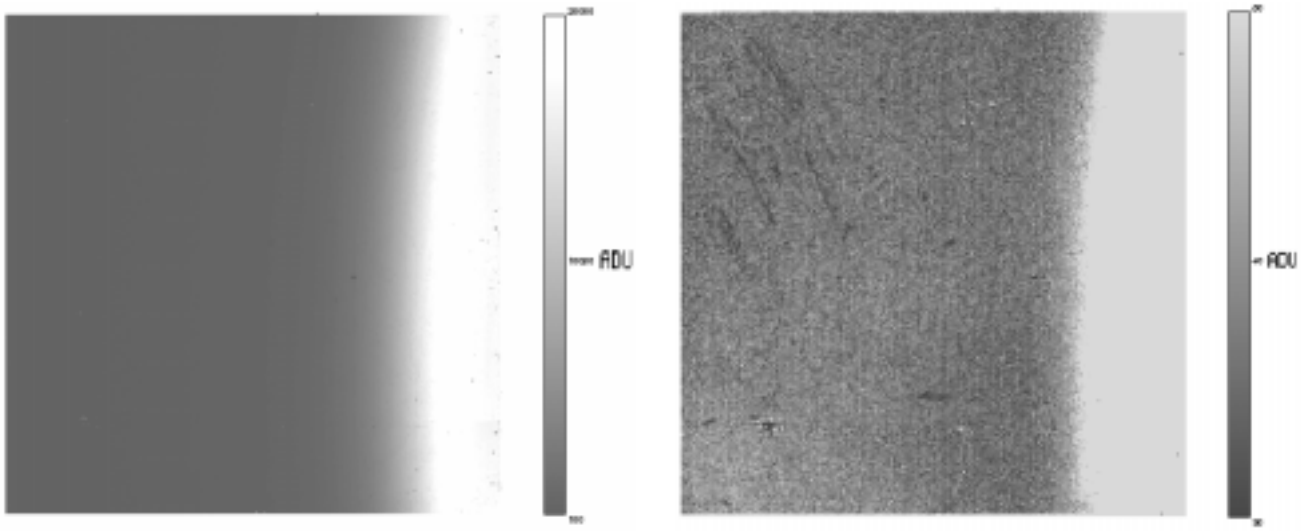

Figure 2. The Source Frame (left) and 1st Latent Image (right). Frames were taken at 450mV of applied reverse bias. The integration time was 16 seconds for the source frame, and 20 seconds for the 1st latent frame.

2.2. Bias and Fluence Coverage

Latent tests were conducted on a series of applied reverse biases and source fluences. The series of biases was selected to give overlapping latent coverage of source flux, fluence, and depletion region width. The series of selected biases ranged from 250mV to 850mV in 100mV steps. Source exposures ranged from 4 seconds to 32 seconds in 4 second steps. At the peak flux in the source frame, 100mV of debiasing corresponded to an increase in integration time of 3-4 seconds.

2.3. Conversion Factor, Linearization, and Well-depth

Conversion factor measurements were made for 3 of the applied biases in the series. Conversion factors from ADUs to electrons were calculated for small signals using the standard signal vs. noise^2 method.[9] For small signals the typical conversion factor was $\sim$7e$^-$/ADU. See Appendix B and figure 11 for a more detailed treatment.

Linearization and well-depth data were taken for 4 of the applied biases in the series. Data was corrected for nonlinear effects due to changes in capacitance at larger signals, See Appendix A.[1] Since the relevant quantities gathered from these measurements are well-behaved and change slowly over bias space, these quantities can be interpolated for biases where they have not been directly measured.

3. DATA ANALYSIS

3.1. Latent image test run

To explore the dependence of latent response to source flux and fluence, boxes representing approximately constant source flux were positioned on the array. The 4 (columns) x 25 (rows) pixel boxes were all centered on row 77.5 and centered on column 2.5 through 253.5, generating 254 box means per frame. Each box overlaps 3 columns with its nearest neighbors. Since the box is oriented such that its length, 25 pixels, is along columns of the array, the average flux and fluence change slowly from one box position to the next. This is a result of choosing the box orientation to match the illumination pattern of the 3.3μm BB filter edge. See Figure 2. The box averages were then linearized and converted to electrons using appropriate factors.

Background flux levels seen on the cd' filter as a small light leak ($\sim$14e$^-$/sec) were determined by taking the box averages of the last 4 latent frames (where the latency has become negligibly small) and averaging them, one for each column position. Subtracting this background removes the light leak from the test data. What remains is only latency and an unavoidable instability level. The instability level is an offset of the entire frame from the zero signal level due, in all likelihood, to instabilities in the bias voltages and/or array temperature changes[‡]. The instability, of typically $\sim$10e$^-$, is corrected by averaging the first 54 columns from the frame, and simply subtracting that average from all boxes in the frame. The first 54 columns are used as they received a negligible amount of flux during the source exposure and therefore should have negligible latency. See Figure 3 for a typical latent test where background and instability have been sequentially removed.

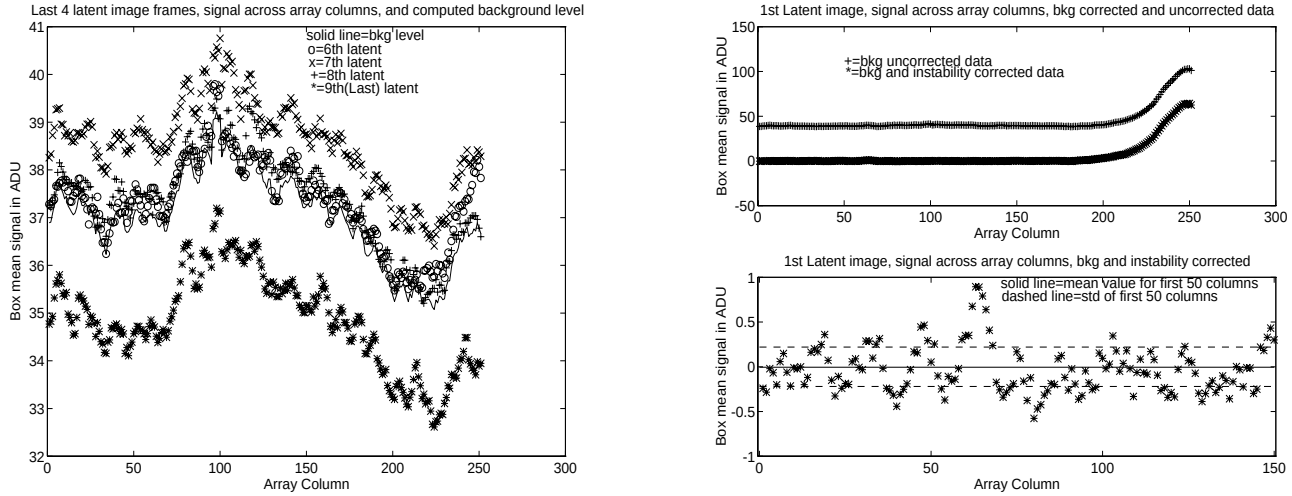

Figure 3. Background and instability corrections to the images. To the left, background levels of the last 4 latent images. The solid line indicates the average background level in the latent test run. It is used to remove the background light level in all frames of the latent test run set. The variation between the levels is attributed to instability. It is the same for the unilluminated columns (1-50), as well as the illuminated columns (200-254). 1 ADU is $\sim$7e$^-$. To the right, background and instability corrected latent test data. Note the signal level falls to zero where no latency is present after background and instability corrections have been performed.

The total latency vector was determined by summing over the box means in the latent frames. The total latency represents the amount of latent charge detected over a $\sim$225 second period as a function of position on the array, (see left figure 4). The ratio of total latency to source fluence versus the detector bias at the end of the source exposure is given in figure 4 on the right. The right side of figure 4 shows that the percentage of latency is an increasing function of the debiasing of the detector. Since the width of the depletion region is a function of detector bias, a dependence of latency on depletion width can be inferred from the figure.

[‡]A temperature change of $\sim$0.01K causes a change in the output voltage of the mux equivalent to $\sim$10e$^-$ of signal.

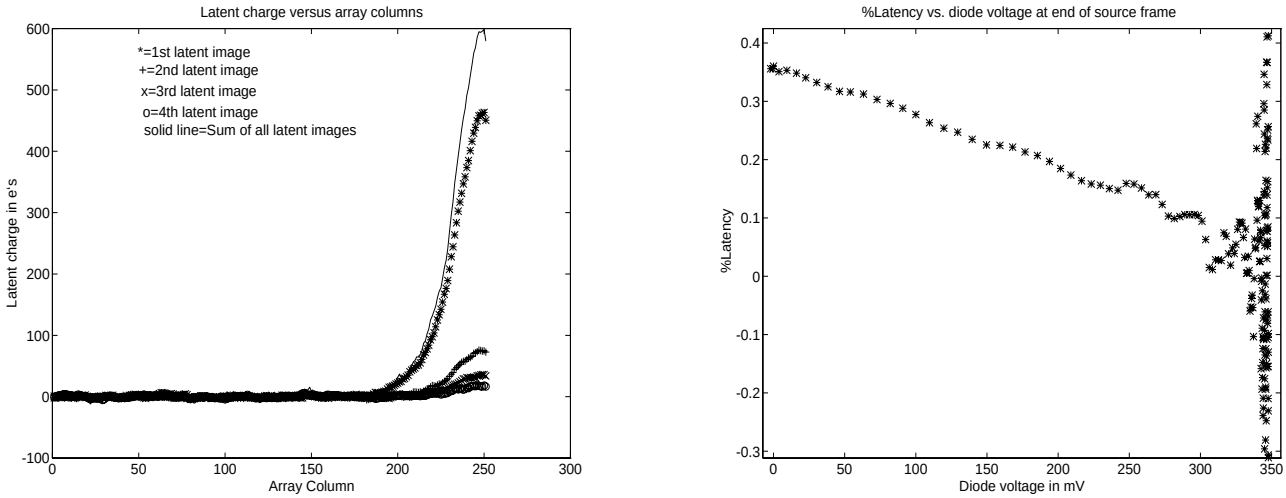

Figure 4. The total latency vector (left), and the %Latency vs. Diode Voltage (right). Only the first 4 latent image signal frames are shown at left, as they comprise the vast majority of the total latency. The Diode voltage, shown at right, is taken at the end of the source frame. All data shown are from the saturation latent test run at 450mV of applied bias.

3.2. Time constants

Previous experiments on similar arrays have shown that fitting the decay of latent signal with time requires at least 3 time constant populations. The total number of traps in each population are comparable. The time constants are typically 1-2s, 20-30s, and 400+s. Here we concentrate on the 20-30s population. The left plot of figure 5 shows a typical exponential fit for the 250mV applied bias test set.[5]

The fitted time constants can then be compared to the source fluence and flux in an effort to determine if a correlation exists. As can be seen in the right plot of figure 5, no correlation between time constant and flux or fluence seems apparent. Furthermore one can see in figure 5 a large scatter of values for smaller fluence. This increased scatter is caused by uncertainty in the fitted time constant when the latency is small.

3.3. Trap Site Numbers

The total latency vector was used to examine the spatial variations in trap site densities. One can compare the width of the depletion region at the end of the source exposure to the corresponding total latent for each test run. The width of the depletion region as a function of reverse bias V of the InSb p-n junction is,

$$w(V) = \sqrt{\frac{2\epsilon\epsilon_o(N_A + N_D)(V_{bi} + V)}{qN_AN_D}} \tag{1}$$

where N_A is the number density of acceptors in the p-type implant, N_D is the number density of donors in the n-type bulk, q is the electron charge, and ϵ is the dielectric constant of InSb.[8]

Since $N_A >> N_D$ equation 1 reduces to,

$$w(V) = \sqrt{\frac{2\epsilon\epsilon_o(V_{bi} + V)}{qN_D}} \tag{2}$$

Depletion widths are calculated using equation 2 and values of 17.7 and $2\text{x}10^{14}\text{cm}^{-3}$ for ϵ and N_D respectively.[3] The reverse bias, V, at the end of the source frame is obtained by subtracting the accumulated charge from the initial reverse bias on the diode. The initial reverse bias applied to the diode can be computed by observing the saturation of a box in the signal frame. Once one box has come to saturation for a given applied bias, then a scaling of the zero

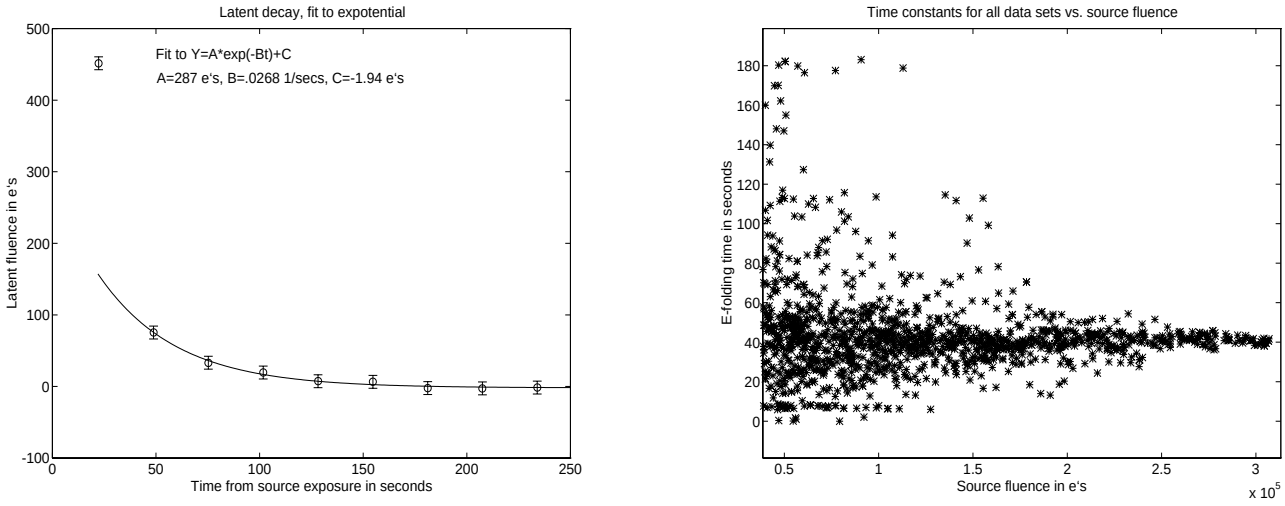

Figure 5. Plot of latency as a function of elapsed time (left), and all time constants from all data sets (right). On the left, data shown is from the 450mV bias test set. Note the 1st latent frame's box mean is omitted from the fit. This is done because traps with time constants shorter then those considered here contribute to the latent signal in the first image. On the right, all time constants whose latent decay fit was obtainable are shown.

bias point determines the initial reverse bias for all boxes. This procedure for determining the initial reverse bias is applied to all test sets. Figure 9 shows the zero bias point at various applied biases. Figure 6 (left) shows the total latent as a function of depletion width for several latent test runs.

One can see from figure 6 (left) that total latency is highly dependant on depletion width. For example, one can see in the 850mV bias test run data, that a 300mV source fluence leads to a total latent of about $\sim 175e^-$, while a 300mV source fluence for the 450mV bias test run data leads to a total latent of $\sim 500e^-$. This implies that the effective populated trap density increases with proximity to the p-type implant.

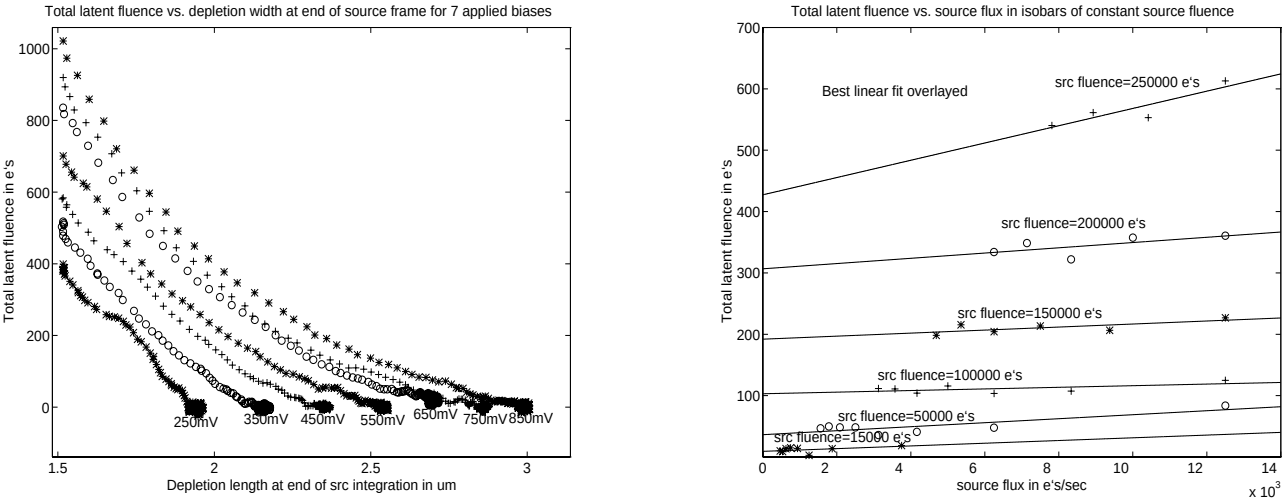

Figure 6. Shown on the left is a plot of the total latency versus depletion region width for several applied biases. The typical uncertainty in the data points is $\sim 40e^-$. Shown on the right is a plot of the total latency versus source flux in isobars of constant fluence. Uncertainty in the data points is at the 10% level. The best linear fit to each isobar of fluence is overlayed. Note total latency increases with increasing flux for constant fluence.

3.4. Latency and source fluence

The spatial density of traps may be inferred by examining total latency as a function of depletion width for data points which share the same flux and fluence.

Linear point to point interpolation of depletion width and total latency for source fluence was used to generate a data set of common fluxes, fluences, depletion widths, and total latents. The interpolation introduces uncertainties that are negligible compared to the 10% uncertainty in the total latency. See figure 7 for an example of the interpolated data points.

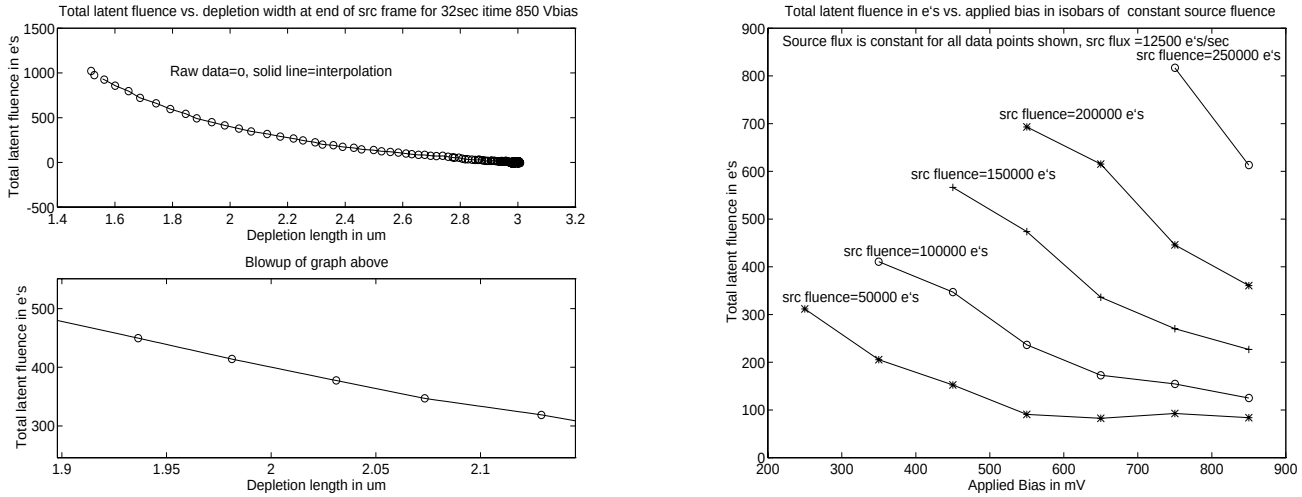

Figure 7. Shown at left is the interpolation of latency, fluence, and depletion width. Uncertainty in the raw data points is at the 10% level. While fluence interpolation is not explicitly shown interpolated values for fluence are used to generate the points that are shown. Shown at right is a plot of total latency versus applied bias. Source flux is constant for all data points shown, 12,500 e^-/sec. Lines of constant fluence are plotted.

Plots of total latency, for constant flux and fluence, as a function of depletion length are given in figure 8 (right). Additionally, one can see a similar plot involving only changes in applied bias, see figure 7 (right). The dependence of trap number on depletion width was fit to an inverse square law, $N(w) = \frac{\alpha}{w^2} + \beta$, see table 1. Other fits were attempted but only the inverse square law yielded acceptable χ^2 values for all fluences.

3.5. Trap Site Density Functions

Based on the inverse square law fit one can derive the spatial distribution of the hole traps under certain geometric assumptions. The geometric assumptions made are explained in more detail in the discussion section. The undepleted volume of n-type material in a pixel as a function of the depletion width is given by (see section 1.2 and figure 1),

$$V_{un}(w) = V_o - (22 + 2w)^2(1 + w)$$

where,

$$V_o = 30^2(7)\mu m^3$$

Hence the differential volume is simply,

$$\frac{dV_{un}(w)}{dw} = -(572 + 184w + 12w^2)$$

and for $w <\sim 4$ the term in w^2 can be neglected. If the traps are distributed throughout the n-type InSb, the total number of trap sites detected will be proportional to the integral of the trap site density function over the undepleted volume of a pixel. If N(w) is the total number of trap sites in the undepleted volume then we have,

$$N(w) = \int_4^w -(572 + 184w)\rho(w)dw$$

Fluence (e^- in thousands)	α ($\mu m^2 e^-$)	β (e^-)	χ^2 (dim)
50	1091	-79	0.90
100	1424	-91	0.25
150	1630	-61	0.44
200	1670	4	1.33

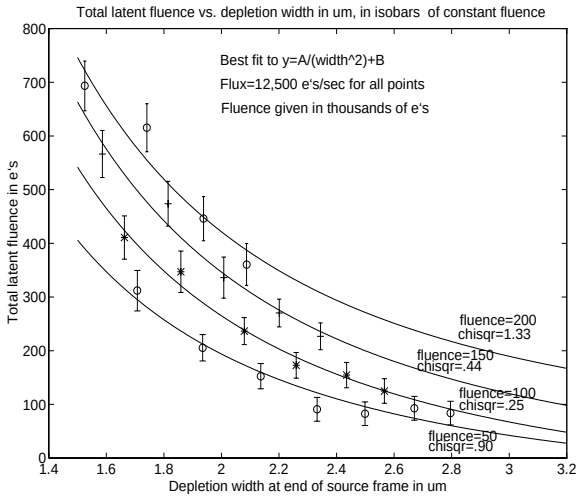

Figure 8. Shown is a table of fit parameters, and a plot of total latency versus depletion width. Source flux is constant for all data points shown, 12,500 e^-/sec. Isobars of constant fluence are plotted. The best fit functional to the data is found to be proportional to the inverse square of the depletion width.

We know from the experimental fit that N(w) falls like an inverse square. Hence,

$$\frac{dN(w)}{dw} \propto \frac{-1}{w^3} \propto -(572 + 184w)\rho(w)$$

Therefore the active trap site density must fall like,

$$\rho(w) \propto \frac{1}{(w^3)(572 + 184w)}$$

Which for values of w between 1.5 and 4μm looks like

$$\rho(w) \sim \frac{1}{w^{3 \leftrightarrow 4}}$$

If the trap sites are located only on the front surface of the InSb, with surface density $\sigma(w)$, then the undepleted front-side area in a pixel as a function of the depletion width is given by,

$$A_{un}(w) = A_o - (22 + 2w)^2$$

where,

$$A_o = 30^2 \mu m^2$$

Hence the differential area is simply,

$$\frac{dA_{un}(w)}{dw} = -(88 + 8w)$$

and for $w <\sim 4$ the term in w can be neglected. Again the best fit gives us for the total number of trap sites,

$$N(w) = \int_4^w -(88)\sigma(w)dw$$

falling like an inverse square. Hence,

$$\frac{dN(w)}{dw} \propto \frac{-1}{w^3} \propto -(88)\sigma(w)$$

Therefore the active trap site surface density must fall like,

$$\sigma(w) \propto \frac{1}{(88)w^3}$$

4. DISCUSSION

Based on the dependence of latent charge on source flux, fluence, and depletion width, we have shown that the total number of active traps follows an inverse square falloff with depletion width. Assuming a trap and pixel geometry, we find that the active trap density falls as the inverse cube of the distance from the p-n junction. We argue that since the time constants are independent of the flux, fluence and depletion width, the same trapping mechanism is at work in all the experiments[§]. Indium oxide was suggested as a possible hole trap species in a previous generation of InSb arrays (SiO_x passivation). These trapping species were hypothesized to be distributed in the passivant within 10-50Å of the InSb/passivation interface. The next generation InSb arrays presented here were passivated with $SiN_{1.3}$, however the new passivation does not preclude the possibility of indium oxide traps. If only these oxide traps were at work in the current generation of arrays then one must explain the apparent rise in active trap density as the depletion width shrinks, or equivalently given our assumed geometry, as one approaches the p-type implants. There are at least 3 possible explanations: 1) trap densities increase with proximity to the p-type implant, 2) traps are preferentially populated closer to the implant, 3) trapped charges closer to the implant are collected more efficiently.

We know damage occurs to the crystalline structure (zincblende)[8] of the n-type bulk during the implantation process, however we are told that this damage is healed during a later annealing process.[3] If impurities are generated by the implantation process then it is difficult to understand how they would be restricted to a small layer near the frontside surface of the detector, however we are told processing methods don't preclude this as a possibility.[7] Additionally, one could argue that the passivating materials are necessary in the activation of the impurities as traps. This leads one to question whether the passivation process itself can cause impurities, oxide or other. If this were the case then the generation mechanism would have to be strongly influenced by the presence of the implant. Since much of the passivating process is proprietary information to Hughes-Raytheon, this possibility cannot be confirmed.

Alternatively, we have seen in a previous generation of detectors the presence of oxide impurities at the fronside surface. If the electrical character of the passivating layer and/or surface InSb were modified upon proximity to the implant, i.e. with decreasing depletion width given our assumed geometry, then hole traps may be generated and/or activated as a result. Additionally, the collection efficiency[¶] itself could be impacted by such an electrical change.

In any case, as a result of the apparent distribution of traps seen here a nominal increase in applied bias will decrease image latency by factors of 2-3.

APPENDIX A.

A.1. Well-depth

The well-depth can be computed by filling the detector's integrating node to capacity. Once this has been done, a simple conversion of the ADU signals to millivolts yields the well-depth, and with the known amount of applied reverse bias, the charge dump (zero bias point), is easily determined.

The well-depths for 4 applied bias sets are determined as functions of position on the array in the same manner introduced in the latent signal section. The ZBP is calculated for each bias set and plotted as a function of its position on the detector in figure 9. Since similar behavior of the ZBP is seen in each bias set, the 450mV bias set is chosen as representative, and the ZBP is scaled for all other applied biases in the image latency calculations.

A.2. Linearization

Since the integrating node of the detector is essentially a capacitor, linearizing signals becomes necessary as charge accumulates. To accomplish this, charge is integrated from a constant source over a variety of integration times. The slope of the integration rate versus total signal curve yields the necessary factor. Signal versus rate data is computed for a box measuring 25 x 25 pixels located near the center of the array. The upper left corner of the box is located at pixel [165,65] The box location is the same for linearity in all bias sets. The best fit linear function for the data is computed for all bias sets. See Figure 9.

[§]This assumes the short time constant traps, which are contained in the first latent image, are generated by the same physical mechanism as the longer time constant traps, implying they have a spatial distribution similar to the longer time-constant traps.

[¶]For our purposes we define the collection efficiency to be the probability of a once trapped then released charge of being collected and counted as photo-charge.

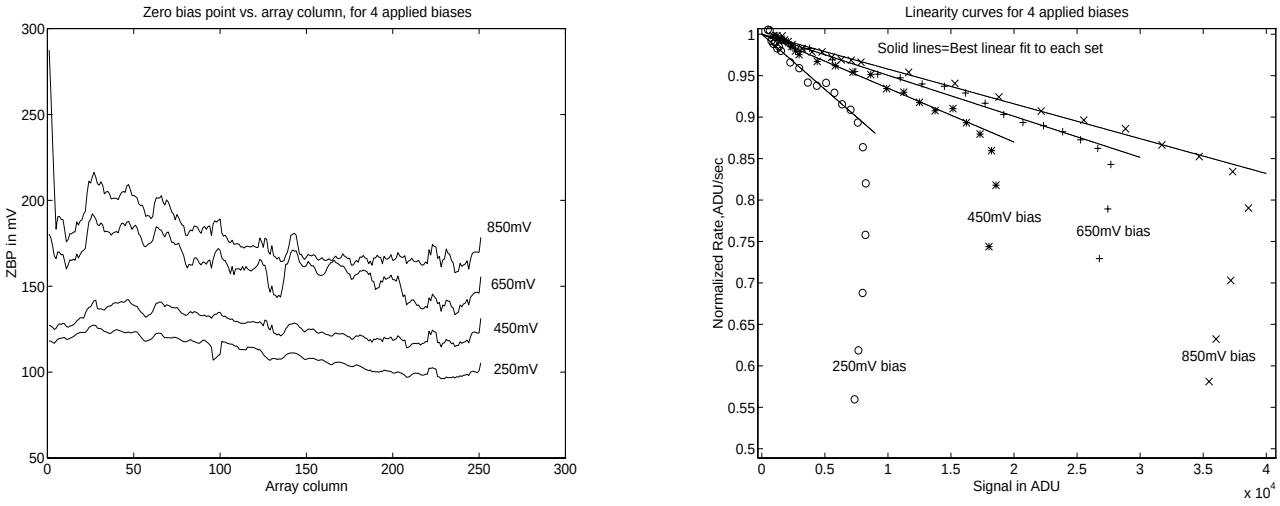

Figure 9. Shown at left are the zero bias points for 4 applied biases. They are plotted versus their position on the array. Shown to the right are linearity curves with best linear fit.

The theoretical signal versus rate curve, from appendix A3, was calculated for each of the 4 applied biases. The predicted linearity curve and the experimental data are shown for the 250mV reverse bias data set. This data set is shown as it reflects the poorest agreement between theory and experimental values, however the theoretical curve still fits the vast majority of the data within their uncertainties. See Figure 10.

A.3. Theoretical derivation of linearity factors.

The detector's capacitance for a given voltage V, is given by,

$$C_{det}(V) = \frac{2C_o}{\sqrt{1+\frac{V}{V_{bi}}}}$$

where C_o ≈.083pF, and V_{bi} ≈235mV , the built in reverse bias.[3]

Now the diode's maximum voltage V_{diode}, is simply the difference between the applied bias and the ZBP. The voltage applied to the integrating node of the detector V, is the difference between V_{diode}, and the equivalent integrated signal voltage, namely,

$$V = V_{diode} - V_{signal}$$

The amount of charge in the integrating node for any given signal is then given by,

$$Q = Q_{diode} - Q_{signal} + C_{fixed+stray}(V_{diode} - V)$$

Changing this to terms of capacitance and voltage we have,

$$Q(V) = (V_{diode} - V_{bi})C_{det}(V_{diode}) - (V - V_{bi})C_{det}(V) + C_{fixed+stray}(V_{diode} - V)$$

The logarithmic derivatives of Q and Signal are observable, and provide the linearity factors,

$$\frac{1}{Lin_{fac}} = \frac{1}{Signal}\frac{Q(V)}{Q(V \approx V_{diode})}$$

Equating these factors with the experimentally derived values for the slope and intercept of the best fit line of signal vs. rate we have,

$$\frac{1}{Lin_{fac}} = \frac{slope}{intercept} Signal + 1$$

substitution yields,

$$\frac{slope}{intercept} = \frac{Q(V \approx V_{diode})}{Q(V)} - \frac{1}{Signal}$$

Finally, substitution for Q(V) into the expression above in terms of voltages yields,

$$\frac{slope}{intercept} = \frac{\sqrt{V_{diode} + V_{bi}} - \sqrt{V + V_{bi}} + r(V_{diode} - V)}{\sqrt{V_{diode} + V_{bi}} - \sqrt{V_{diode} + V_{bi} - N} + rN} - \frac{1}{s} \,, \tag{3}$$

where,

$$r = \frac{C_{fixed+stray}}{2\, C_o \sqrt{V_{bi}}}$$

and,

$$N = \frac{S_o\, C_{ADU/e}}{Gain * Dcgain}$$

The constant N is a signal voltage for signals, $S_o \sim 0$. This factor scales the linearity factors to unity in the low signal level regime.

A.4. Experimental linearity factors

Theoretical linearity factors (equation 3), are fit to the experimental data using a regressive best fit algorithm. The theoretical value for the constant A can be determined from its definition, however, to obtain a reasonable fit to the data, the algorithm is allowed to fit the normalization condition.

Once any given signal level is chosen, the values of s and V, are fixed. No one choice of signal level is preferable to any other however, one must keep in mind that the signal level chosen can not exceed the well-depth of the smallest applied bias. Since our smallest applied bias gives a well-depth of approximately 150mV, a signal level of 100mV of well is chosen. To ensure the fitting algorithm is working properly the fraction $\frac{1}{s}$ is fit as well as the normalization constant N. The algorithm returns a value for the fraction approximately equal to 100mV of signal, as one would expect. A plot of linearization factors as predicted by the best fit to the theory, and the experimental data points is shown in figure 10 (right). Since the theory fails to predict 2 of the 4 data points shown on the plot within their experimental uncertainties, the theory is not used for interpolation of linearity factors for other biases in the experiment. A simple point to point cubic fit, a spline, is used to interpolate the linearity for other biases.

APPENDIX B.

B.1. Capacitance and Conversion Factor

Interpolating ADU's to actual numbers of charge carriers in the integrating node requires measurements of signal and the associated shot noise. An adequate amount of photo-signal is required so that the shot noise dominates the mux's readnoise. Since the readnoise is approximately 30 e^- for 1 fowler pair, one should have at least 2000 e^- of signal to begin dominating the readnoise[‖]. Of course, one would continue with larger signals to be certain of shot noise domination, but linearization effects can become significant if signal variance is large. The slope of the curve of signal vs. noise^2 then yields the proper conversion factor for e^- per ADU.

Conversion factors are calculated for 3 applied bias test sets. In each test set 3 boxes are positioned on the array, each box measuring 25x25 pixels square. The boxes are positioned such that they do not overlap, and do not

[‖]Assuming a Poisson distribution for the integrated signal

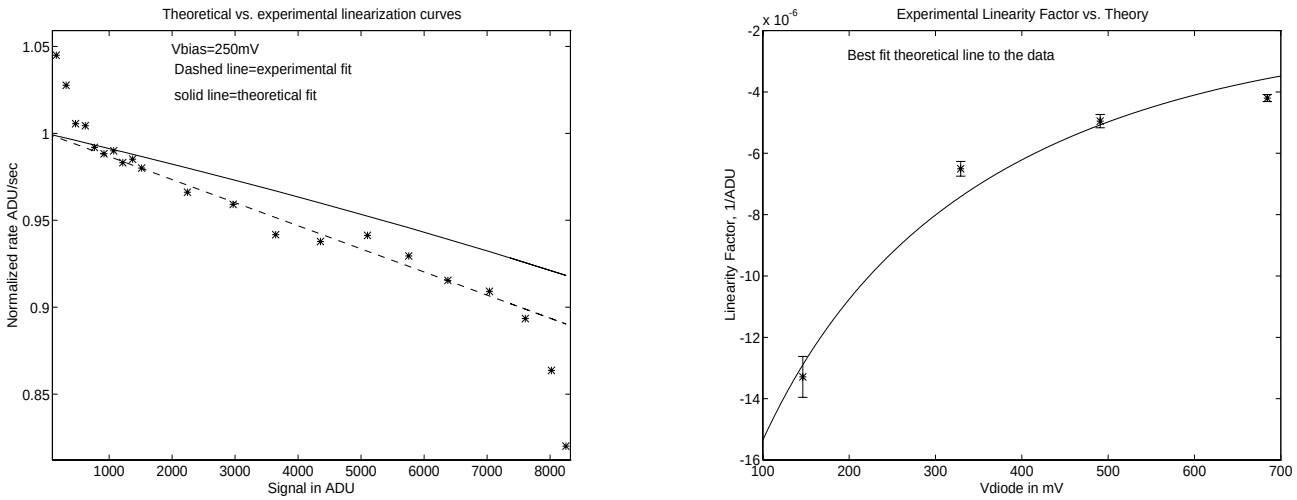

Figure 10. Shown to the left is a plot of linearization curves, theory vs. experimental. The 250mV bias data set, the worst agreement between theory and experimental values is shown. Short integration times and saturated boxes have been omitted for clarity. Shown to the right are the linearity factors, theory and experimental values. The factors are calculated for 100mV of fluence.

include hot pixels. The best linear fit to noise^2 versus signal for a given box from the 250mV bias test set is shown in figure 11 as an example, note only the filter wheel position is changed from data point to data point, to increase photo-signal**.

The boxes are averaged for each bias set and standard deviations computed. The experimental values are then compared to the theoretical values.

B.2. Theoretical derivation of conversion factors.

The integrating node's capacitance for a given diode voltage may be seen to be,

$$C_v = A_d \sqrt{\frac{\epsilon\epsilon\epsilon_o}{2\frac{V_{bi}+V_{diode}}{N_D}}}$$

where A is the equivalent area of the capacitor,[1] e is the charge of an electron, ϵ_o is the dielectric constant of the n-type InSb, and N_D is the donor concentration in the n-type.

The total capacitance is then just a linear sum of the mux's fixed capacitance and the integrating node's capacitance,

$$C_t = C_{mux} + C_v$$

The conversion factor is simply a scaling of the capacitance with the A/D boards and appropriate gain factors,

$$C_{fact} = C_t\left(\frac{10}{2^{15}\, dcgain * gain * \epsilon}\right)$$

Substitution yields,

$$C_{fact} = \frac{A}{\sqrt{V_{bi}+V_{diode}}} + B$$

**The wavelength range wherein data is collected does not exceed the minimum energy required to collisionally excite holes. Namely, there is no signal gain due to collisionally excited charge.

where,

$$A = \frac{10\,A_d}{2^{15}\,gain * dcgain * e}\sqrt{\frac{N_D\,\epsilon\,\epsilon\,\epsilon_o}{2}}\;,\; and\; B = \frac{10\,C_{mux}}{2^{15}\,gain * dcgain * e}$$

B.3. Experimental conversion factors

A best fit algorithm is employed to determine A and B, and the results are plotted in figure 11. Using the best fit values for the constants, the effective area of the capacitor is $455\mu\mathrm{m}^2$ and the fixed capacitance of the mux is .035pF. Since the theory fits the experimental results very well, the values of the conversion factors for other biases in the experiment will be determined by the theoretical best fit.

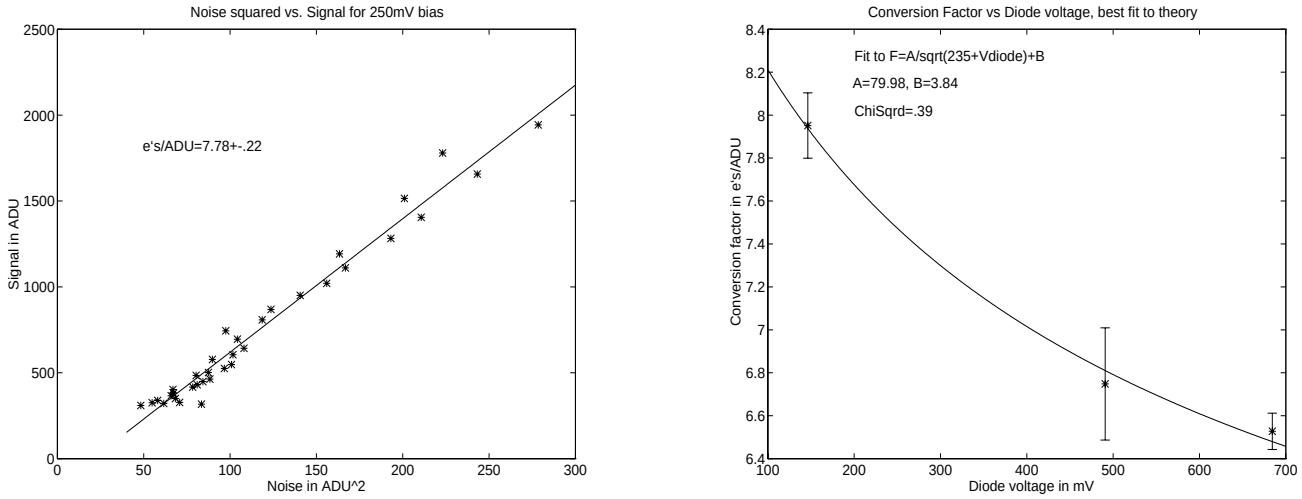

Figure 11. Plotted to the left is the best linear fit which determines the conversion factor. Fit are the 25x25 pixel square box means versus their respective noise^2 as computed from the difference of 2 successive signal frames. Shown at right is the best theoretical fit for conversion factors to the experimental data as a function of the applied reverse bias.

APPENDIX C.

C.1. Latent performance of IRAC's Insb Arrays.

The two IRAC Insb arrays were tested for image latency at the University of Rochester. SCA 48534 (IRAC ch1) was tested on october 27, 1998, and SCA 48975 (IRAC ch2) was tested on february 17, 1999. At the time they were tested the Insb arrays had not yet received their flight mounts and were mounted on leadless chip carriers. See the paper submitted at this conference by Pipher et al. A summary of results is given in the table in figure 12.

Test number	Flux (e^-/sec)	Exposure Time(secs)	Delay Time(secs)	Integration Time(secs)	Required latent Fluence(e^-)	IRAC ch1 Fluence(e^-)	IRAC ch2 Fluence(e^-)
1	2500	20	0	20	10	72	25
2	2500	20	200	20	1	3	2

Figure 12. Shown are the latent image requirements and results for the IRAC Insb's for SIRTF. The delay time is the time between the end of the source exposure and the beginning of first latent image. The integration time is quoted for the latent image.

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